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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,509	05/24/2001	Lee D. Whetsel	TI-31076	2438

23494 7590 08/17/2005

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/864,509	WHETSEL ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 and 306 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on May 27, 2005 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Response to Arguments

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Nadeau-Dostie et al. U.S. Patent No. 6,000,051.

As per claim 1, Nadeau-Dostie et al. teach a process of selecting different 1149.1 TAP domain arrangements within an integrated circuit comprising: performing an 1149.1 instruction shift operation through a first 1149.1 TAP domain arrangement, performing an 1149.1 instruction update operation at the end of said 1149.1 instruction shift operation, and; in response to said 1149.1 instruction update operation, selecting a second 1149.1 TAP domain arrangement which differs from the first 1149.1 TAP domain arrangement. In which, a method of testing high speed interconnectivity of circuit boards having components operable at a high speed system clock, employing an IEEE 1149.1 standard test method in which test data is shifted into and from the components at the rate of a test clock during Shift.sub.-- In and Shift.sub.-- Out operations, and having an Update operation and a Capture operation between the Shift.sub.-- In and Shift.sub.-- Out operations, the components including a first group of components capable of performing the Update and Capture operations at the rate of the Test Clock only and a second group of components capable of performing the Update and Capture operations at the rate of the system clock, the method comprising the steps of performing the Shift.sub.-- In operation in all of the components concurrently at the rate of the Test Clock; performing the Update and Capture Operations in the first group of components at the rate of the Test Clock; and performing the Update and Capture Operations in the second group of components at the rate of the system Clock (Abstract). For each system clock domain, a separate synchronize signal 114 is generated. The same integrated circuit can generate multiple synchronize signals. The high-speed mode of interconnect test can be active for all system clocks at the same

time as long as no signal is going from one system clock domain to another. Of course, it is allowed to go in and out of the low speed test clock domain to or from a system clock domain. If signals cross the system clock domain boundaries, the high-speed interconnect test mode can only be activated on a subset of the system clock domain at a time so that the condition is met (column 13 line 61 through column 14 line 6).

As per claim 3, Nadeau-Dostie et al. teach the use of IEEE 1149.1 standard to perform an instruction shift operation, employing an IEEE 1149.1 standard test method in which test data is shifted into and from the components at the rate of a test clock (Abstract).

As per claim 4, Nadeau-Dostie et al. teach employing IEEE 1149.1 standard test methods in which test data is shifted into and from the components at the rate of a test clock during Shift.sub.-- In and Shift.sub.-- Out operations, and having an update operation and a capture operation between the Shift.sub.-- In and Shift.sub.-- Out operations, the improvement comprises executing the update and capture operations at the rate of the system clock.

As per claim 5, Nadeau-Dostie et al. teach performing a select DR operation, a select TR operation, and a capture IR operation before performing the instruction shift operation. (Column 6 lines 22-40).

As per claim 6, Nadeau-Dostie et al. teach performing one of a select DR operation and a Run Test/Idle operation after performing the instruction update operation. (Column 6 lines 10-40).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 6,587,981 Mauradali et al.

This patent teaches a scan path structure for integrated circuits, which contain one or more cores or levels of sub-cores, embedded within the costs. Circuitry is provided to permit scan testing of scan elements, such as scan wrapper cells and scan chains, in the cores and sub-cores by providing scan paths which share access to limited numbers of scan test ports of the integrated circuit under test.

U. S. Patent No. 6,658,614 Nagoya

This patent teaches he boundary scan elements have the input-terminal-side boundary cells and output-terminal-side boundary cells connected in parallel between the TDI terminal and the TDO terminal, communication data can be directly transferred to the respective-terminal-side boundary cells via the TDI terminal and the TDO terminal. Therefore, communication data can be transferred at a greater transfer rate than by means of a communication system in which all boundary cells are connected in series.

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on May 27, 2005 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS**

MADE FINAL. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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